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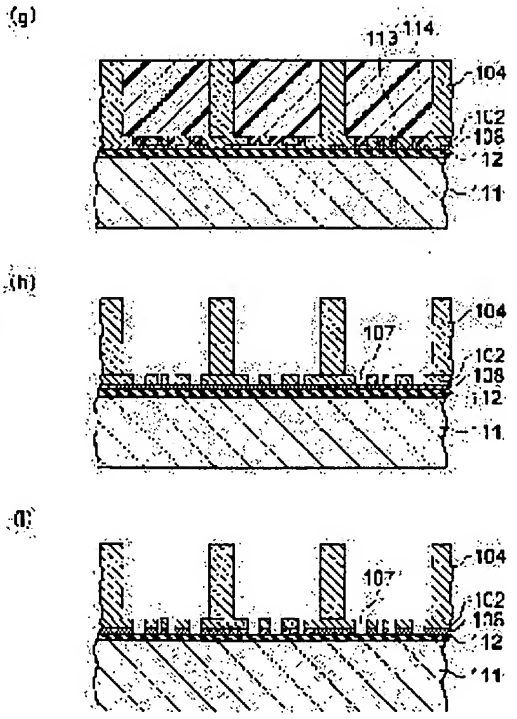
(54) MASK, MANUFACTURING METHOD THEREOF AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a mask, a manufacturing method thereof and a semiconductor device manufacturing method which raises the efficiency of the mask manufacturing and improves the machining precision of patterns.

SOLUTION: The mask manufacturing method comprises a step of laminating a sacrificial film 112 and a conductive layer 108 on a substrate 111, a step of forming a metal film 102 having apertures 107 by electroplating and electrolytic polishing with a resist 113 used for a mold, a step of forming a metal film support (strut) 104 by electroplating and electrolytic polishing with a resist 114 used for a mold, a step of removing the resists 114, 113, a step of removing the conductive layer 108 on at least the apertures 107, and a step of removing the sacrificial film 112 to separate the substrate 111. The mask is thus manufactured and a semiconductor device is manufactured, using the same.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a mask for electron beam transcription mold lithography and a manufacturing method for the same, and the manufacturing method of the semiconductor device using it especially about a mask for lithography and a manufacturing method for the same, and the manufacturing method of the semiconductor device which uses it.
[0002]
[Description of the Prior Art]The resolution of the optical lithography used as a means of LSI pattern formation is approaching the limit with progress of the minuteness making of LSI, and high integration. The electron beam lithography which has high potential to minuteness making as a means replaced with optical lithography attracts attention.
[0003]Although it was that the greatest problem of electron beam lithography has low throughput conventionally, The mask for transfer called a stencil mask is produced beforehand, the electron beam package projection exposure method which carries out projection transfer of this mask pattern on a wafer was proposed, and the prospect which can also solve this problem came out.
[0004]As an electron beam package projection exposure method with which utilization is advanced, For example, PREVAIL ("Projection reduction exposure with variable axis immersion lenses:Next generation.) which IBM and NIKON are developing jointly Journal of Vacuum Science and Technology B17 p.2840 (1999) besides lithography"/H.C. Pfeiffer are mentioned. .SCALPEL which Lucent Technologies etc. are developing. (scattering with angular.) Proceedings of SPIE 3676 p.194 (1999) besides limitation in projection electron-beam lithography/S.T.Stanton are mentioned.
[0005]The schematic diagram of the stencil mask used for the above electron beam

lithography is shown in drawing 8 (a). Drawing 8 (b) is the perspective view which expanded a part of drawing 8 (a) (A). As shown in drawing 8 (a), the stencil mask 201 is formed considering the silicon wafer 202 of 8 inch sizes as a base. The silicon wafer 202 has two or more membrane parts (membrane) 203 with a size of 1.13 mm x 1.13 mm, for example. The membrane 203 is mutually separated by the beam called the strut 204. The width of the strut 204 between the membranes 203 is 170 micrometers. The strut 204 acts as a base material which maintains the mechanical strength of the stencil mask 201.

[0006]As shown in drawing 8 (b), the thickness of the membrane 203 is 2 micrometers. When forming the stencil mask 201 using an 8-inch wafer, the height of the strut 204 is almost equal to the thickness of a wafer, for example, is set to 725 micrometers. The membrane 203 contains the margin called the pattern space 205 and the skirt board 206 of the circumference of 1 mm square with which an electron beam is irradiated. The aperture corresponding to an LSI mask pattern is formed in the pattern space 205.

[0007]Drawing 9 is some (X-X') sectional views of drawing 8 (a). The aperture 207 is formed in the pattern space of the membrane 203 as shown in drawing 9. The silicon oxide 209 is formed between the silicon layer 208 containing the membrane 203 and the strut 204. In the process of etching into the rear face of the silicon wafer 202, and forming the strut 204, the silicon oxide 209 is used as an etching stopper layer.

[0008]When performing electron beam lithography of a package projection exposure method like PREVAIL or SCALPEL, the membrane 203 side of the stencil mask 201 of drawing 9 is irradiated with the electron beam of about 100 keV, for example. The electron beam irradiated by the membrane 203 penetrates only aperture 207 portion to the strut 204 side by no being scattered about, and converges on resist. PREVAIL and SCALPEL(s) are usually 4 times as many reduction projection systems.

[0009]The manufacturing method of the above stencil masks 201 is explained below with reference to drawing 10. First, as shown in drawing 10 (a), the SOI wafer 211 is produced. In one field of the silicon wafer 202, the SOI wafer 211 has the silicon layer 208 via the silicon oxide 209, and has the rear-face side silicon oxide 212 in it in the field of another side of the silicon wafer 202. The SOI wafer 211 can be formed by for example, the SIMOX (separation by implanted oxygen) method or a lamination method.

[0010]Next, as shown in drawing 10 (b), the resist 213 is formed in the rear-face side of the SOI wafer 211 by the pattern (refer to drawing 8) of a strut. After applying the resist 213 to the whole surface with a spin coat, it forms by performing exposure and development. Dry etching is performed to the rear-face side silicon oxide 212 and the silicon wafer 202 by using resist 213 as a mask from the rear-face side of the SOI wafer 211. Thereby, the strut 204 which consists of silicon is formed.

[0011]Next, as shown in drawing 10 (c), it etches into the silicon oxide 209 by the side of the

surface by using the strut 204 as a mask. Then, the resist 213 is removed. Next, as shown in drawing 10 (d), the resist 214 of a predetermined pattern is formed on the silicon layer 208. Then, dry etching is performed to the silicon layer 208 of membrane 203 portion by using resist 214 as a mask.

[0012]Thereby, as shown in drawing 9, the membrane 203 which has the aperture 207 of a predetermined pattern is formed. Then, the rear-face side silicon oxide 212 and the resist 214 are removed. The stencil mask 201 is formed of the above process.

[0013]

[Problem(s) to be Solved by the Invention]However, according to the manufacturing method of the above-mentioned conventional mask, there is a problem that the etching process of the silicon wafer 202 for forming the strut 204 takes a long time. Several hours are required in order to perform dry etching for the thickness of the silicon wafer 202.

[0014]If the strut 204 is beforehand formed as shown in drawing 10 (b) or (c) before a design pattern is completed, mask strength will fall remarkably and it will become easy to damage a mask during storage of a mask or conveyance. In order to avoid the fall of the yield by this, etching of the silicon wafer 202 is usually started after the end of a design pattern. Therefore, shortening of the turn around time (TAT) from the end of a design pattern to mask completion is difficult.

[0015]According to wet etching, it is more possible than dry etching to etch a part for the thickness of the silicon wafer 202 for a short time, but vertical processing like dry etching cannot be performed. If an opening is formed in the silicon wafer 202 by wet etching, the caliber by the side of the rear face of the silicon wafer 202 will become larger than the caliber in the surface by the side of the membrane 203 of the silicon wafer 202.

[0016]Thus, since a section serves as tapered shape according to wet etching, as compared with the case where it is dry etching, the width of the strut 204 becomes large. For example, in the case of electron-beam lithography of a reduction projection system like PREVAIL or SCALPEL, the stencil mask 201 is clustered in matrix form, and it is necessary to form the membrane 203 in it. Since the width of the strut 204 will become large and the area of the field which can be used as the membrane 203 will become narrow if the strut 204 is formed by wet etching, the mask sizes corresponding to the chip size of LSI are no longer obtained.

[0017]According to the manufacturing method of the above-mentioned conventional mask, after performing etching from the rear-face side of the silicon wafer 202 and forming the strut 204, the resist of an LSI mask pattern is formed in the surface side of the silicon wafer 202. Therefore, when forming the resist 214 in the surface side of the silicon wafer 202, it is necessary to perform alignment from the both-sides side of the silicon wafer 202. It is comparatively difficult to perform alignment from both sides with high precision, and the yield of a mask falls easily. A double-sided aligner is also required.

[0018]According to the manufacturing method of the above-mentioned conventional mask, after applying resist to the surface side of the silicon wafer 202, the baking powder of resist becomes uneven easily. Baking powder lays the silicon wafer 202 on a hot plate, and is performed. Since the silicon wafer 202 is supported by the strut 204 at this time, heat conduction from a hot plate becomes uneven in a wafer surface. When baking powder becomes uneven, the process tolerance of a pattern falls.

[0019]As a method of solving such a problem, how to provide unevenness in the hot plate surface can be considered, for example so that it may correspond to the pattern of a strut, but it is expected that the mechanism of temperature control is complicated or the flexibility of a device falls, and realization is difficult.

[0020]Also when performing dry etching to the silicon layer 208 and forming the aperture 207, the original recording of the stencil mask 201 is supported by the strut 204. Therefore, a crevice is formed between the membrane 203 and the stage of an etching device.

[0021]Thus, in the state where the mechanical strength of the whole mask fell, if the influence of generation of heat at the time of etching, etc. is added, in being the worst, it will damage a mask. Even if a mask is not damaged, if a mask changes by generation of heat at the time of etching, etc., the membrane 203 will no longer be supported stably. Thereby, the process tolerance of a pattern falls or a pattern dimension shows dispersion.

[0022]In order to solve such a problem, how to provide unevenness in the stage of an etching device can be considered like the case of the baking powder of resist mentioned above, but since it is the same, realization is difficult. In addition to an above-mentioned resist baking process and etching process, it exposes to resist and the same problem occurs also in the process of drawing an LSI mask pattern.

[0023]The manufacturing method which can avoid the problem resulting from the mask of a manufacturing process being supported by the strut among the above problems is also proposed. According to this method, after forming an aperture in a membrane previously using a SOI wafer in a similar manner, a membrane is protected by resist etc. and etching of a silicon wafer, i.e., formation of a strut, is performed later.

[0024]However, when the dry etching process of the silicon wafer which requires a long time exists also by this method, shortening of TAT from the end of a design pattern to mask completion is difficult. When removing the resist which protects a membrane, the surface of a membrane may receive damage. When a stencil mask is used in electron beam lithography, an electron beam will serve as a defect of a mask pattern, if especially the edge of an aperture receives damage, since it glares from the membrane side.

[0025]When an aperture is formed in a membrane by dry etching besides the above-mentioned problem, there is also a problem that the edge roughness of an aperture increases easily. Since an electron beam is irradiated from the membrane side, if the edge roughness of

an aperture increases, it will become a defect of a mask pattern.
[0026]This invention is made in view of the above-mentioned problem, and is a thing.
The purpose is to provide a mask which this invention raises the efficiency of mask manufacture, and can improve the process tolerance of a pattern, and a manufacturing method for the same.
An object of this invention is to provide the manufacturing method of the semiconductor device which can raise the manufacturing efficiency and the yield of a semiconductor device by including the lithography process which uses the above-mentioned mask.
[0027]
[Means for Solving the Problem]This invention is characterized by a mask comprising the following, in order to attain the above-mentioned purpose.
Metal thin film.
An aperture formed in said some of metal thin films which make a charged particle beam or electromagnetic waves which are irradiated at the 1st page side of said metal thin film penetrate to the 2nd page side locally.
A metal thin film supporting part which was formed in a part on said 2nd page of said metal thin film so that a charged particle beam or electromagnetic waves which penetrated said metal thin film might not be intercepted and which consists of metallic materials.

[0028]A mask of this invention has a conductive layer further on said 1st page of said metal thin film suitably, and said conductive layer has an aperture which said charged particle beam or electromagnetic waves penetrate in the almost same position as an aperture of said metal thin film. Said charged particle beam of a mask of this invention is an electron beam or an ion beam suitably, and said electromagnetic wave is EUV light or X-rays. A mask of this invention is shape in which said metal thin film supporting part was arranged by matrix form on said 2nd page of said metal thin film and which has two or more rectangular openings suitably.
[0029]This becomes possible to form a strut (metal thin film supporting part) in a stencil mask for lithography, without performing dry etching for thickness of a silicon wafer, and the time required of mask manufacture can be shortened. Where a membrane (metal thin film) is supported only by a strut, it becomes unnecessary to perform etching, lithography, etc. and process tolerance of an aperture improves.
[0030]This invention is characterized by a manufacturing method of a mask comprising the following, in order to attain the further above-mentioned purpose.
A process of forming a conductive layer in one field of a substrate.
A process of forming the 1st sacrificial film in a part on said conductive layer.
A process of forming the 1st metal layer that covers said 1st sacrificial film on said conductive layer with electrolysis plating.

A process of forming a metal thin film which grinds said 1st metal layer until said 1st sacrificial film is exposed, and has an aperture into said 1st sacrificial film portion, With a process of forming the 2nd sacrificial film thicker than said 1st sacrificial film in a part on said metal thin film which contains said aperture part at least, and electrolysis plating. A process of forming the 2nd metal layer that covers said 2nd sacrificial film on said metal thin film, A process of grinding said 2nd metal layer until said 2nd sacrificial film is exposed, and forming a metal thin film supporting part, a process of removing said 2nd sacrificial film, a process of removing said 1st sacrificial film, a process of removing said conductive layer of said aperture part at least, and a process of removing said substrate.

[0031]A process at which a manufacturing method of a mask of this invention grinds said 1st and 2nd metal layers suitably includes an electrolytic-polishing process. A process of a manufacturing method of a mask of this invention having further suitably the process of forming the 3rd sacrificial film between layers of said substrate and said conductive layer before forming said conductive layer, and removing said substrate includes a process into which said substrate is made to separate from said mask by removing said 3rd sacrificial film.
[0032]A process in which said substrate is a silicon substrate and a manufacturing method of a mask of this invention forms said 3rd sacrificial film suitably includes a process of forming silicon oxide in the surface of said silicon substrate. A process in which a manufacturing method of a mask of this invention forms said 1st and 2nd sacrificial films suitably includes a process of forming resist with lithography. A manufacturing method of a mask of this invention makes said substrate separate from said mask by removing said whole conductive layer suitably in a process of removing said conductive layer of said aperture part at least.
[0033]This becomes possible to form a strut (metal thin film supporting part) in a stencil mask for lithography, without performing dry etching for thickness of a silicon wafer, and the time required of mask manufacture can be shortened. Where a membrane (metal thin film) is supported only by a strut, it becomes unnecessary to perform etching, lithography, etc. and process tolerance of an aperture improves.
[0034]According to the manufacturing method of a mask of this invention, since damage to that step coverage nature and an embedding characteristic of electrolysis plating are high and an aperture edge by dry etching can be prevented, edge roughness of an aperture falls and a defect of a mask pattern can be reduced.
[0035]Furthermore, this invention in order to attain the above-mentioned purpose a manufacturing method of a semiconductor device of this invention, A process of forming a mask for lithography which has a predetermined mask pattern, An exposure surface is irradiated with a charged particle beam or electromagnetic waves via said mask for lithography, and a manufacturing method of a semiconductor device which has the process of

transferring said mask pattern to said exposure surface is characterized by comprising the following:
A process at which a process of forming said mask for lithography forms a conductive layer in one field of a substrate.
A process of forming the 1st sacrificial film in a part on said conductive layer.
A process of forming the 1st metal layer that covers said 1st sacrificial film on said conductive layer with electrolysis plating.
A process of forming a metal thin film which grinds said 1st metal layer until said 1st sacrificial film is exposed, and has an aperture into said 1st sacrificial film portion, With a process of forming the 2nd sacrificial film thicker than said 1st sacrificial film in a part on said metal thin film which contains said aperture part at least, and electrolysis plating. A process of forming the 2nd metal layer that covers said 2nd sacrificial film on said metal thin film, A process of grinding said 2nd metal layer until said 2nd sacrificial film is exposed, and forming a metal thin film supporting part, a process of removing said 2nd sacrificial film, a process of removing said 1st sacrificial film, a process of removing said conductive layer of said aperture part at least, and a process of removing said substrate.

[0036]Since the time required for manufacturing a mask for lithography is shortened by this, and a mask pattern defect decreases and a yield of a semiconductor device improves, a manufacturing cost of a semiconductor device is reduced. Since pattern processing accuracy of a mask for lithography improves, it becomes possible to transfer a minute pattern with high precision on an exposure surface.
[0037]
[Embodiment of the Invention]Below, the embodiment of a mask of this invention, and the manufacturing method and the manufacturing method of a semiconductor device for the same is described with reference to drawings.
(Embodiment 1) The mask of this embodiment is replaced with the conventional silicon system material, and is formed using a metallic material. Drawing 1 and drawing 2 are the figures showing feasibility [of a metal system stencil mask]. In drawing 1 and drawing 2, although chromium (Cr) is made into the example, other simple substance metal and alloys are also realizable.
[0038]Drawing 1 compares generation of heat by the exposure of an electron beam with silicon and chromium, sets energy of the electron beam at the time of outgoing radiation to 1, and the result of having estimated the rate (rate of energy-absorbing) of the energy accumulated in a membrane is shown. If the rate of energy-absorbing becomes large, generation of heat will also become large. It is proved by the rate of energy-absorbing in case the thickness of silicon membrane is 2 micrometers that the influence of generation of heat can be disregarded.

[0039]In the paper (J. Vac. Sci. Technol. B17 p.2840) besides H.C. Pfeiffer (1999) mentioned above. A mask pattern is transferred using the stencil mask which has the silicon membrane of 2-micrometer thickness, and the example in which the resist pattern was formed is indicated. The thickness of the chromium membrane used as the rate of energy-absorbing comparable as the silicon membrane of 2-micrometer thickness is presumed to be about 0.7 micrometer. When membrane thickness is equal, it is a cause that that the rate of energy-absorbing becomes large rather than silicon membrane in the chromium membrane has respectively the atomic weight and density of chromium larger than the atomic weight and density of silicon.
[0040]If membrane thickness becomes thin, distortion of a membrane will pose a problem. Drawing 2 estimates the amount of deflections of the membrane by gravity in the center section of the membrane of 1 mm square. A deflection becomes large, so that a membrane becomes thin, as shown in drawing 2. In the case of the chromium membrane of 0.7-micrometer thickness, it is expected that a little less than 1-nm deflection which is about 10 times the silicon membrane of 2-micrometer thickness occurs.
[0041]However, if the amount of deflections of a membrane is about 10 nm, as an error factor of electron beam optical systems, It is reported that it is in tolerance level (J. A.). Liddle and H.A. Huggins. and G.P. Watson and "Error. budget analysis of the SCALPEL mask for sub-0.2 micron lithography", J. Vac. Sci. Technol., and B13 p.2483 (1995). Therefore, the amount of deflections of the grade generated in the chromium membrane of 0.7-micrometer thickness does not pose a practical problem.
[0042]Although the metal which has an atomic weight and density comparable as chromium from the above thing is demanded [to thin-film-ize from a viewpoint of generation of heat to around 1 micrometer], if it is membrane thickness of this level, it can be said that the amount of deflections is in tolerance level, and is applicable as a stencil mask material.
[0043]Next, a mask of this embodiment and a manufacturing method for the same are explained with reference to drawings. Drawing 3 (a) is a schematic diagram of the stencil mask of this embodiment, and drawing 3 (b) is the perspective view which expanded a part of drawing 3 (a) (A). The stencil mask 101 of this embodiment is used for the electron beam lithography of a reduction projection system like PREVAIL, for example.
[0044]As shown in drawing 3 (a), the stencil mask 101 is formed, for example considering the wafer form chromium layer 102 of 8 inch sizes as a base. The chromium layer 102 contains two or more membrane parts (membrane) 103 with a size of 1.13 mm x 1.13 mm, for example. The membrane 103 is mutually separated by the beam called the strut 104. The width of the strut 104 between the membranes 103 is 170 micrometers. The neighborhood of an edge of the chromium layer 102 in which the membrane 103 is not formed is also thick-film-ized by the strut 104. The strut 104 acts as a base material which maintains the mechanical strength of the stencil mask 101.

[0045]As shown in drawing 3 (b), the thickness of the membrane 103 is 1 micrometer. According to the stencil mask 101 of this embodiment, unlike the conventional stencil mask mentioned above, the strut 104 changes to silicon and is formed using chromium. Therefore, height h of the strut 104 can be arbitrarily set up regardless of the thickness of a silicon wafer in the range in which the mechanical strength of the stencil mask 101 is maintained. The membrane 103 is provided with the following.
The pattern space 105 of 1 mm square with which an electron beam is irradiated.
The margin called the skirt board 106 of the circumference.
The aperture corresponding to an LSI mask pattern is formed in the pattern space 105.
[0046]Drawing 4 (a) is some (X-X') sectional views of drawing 3 (a). The aperture 107 is formed in the pattern space of the membrane 103 as shown in drawing 4 (a). The strut 104 which consists of chromium, for example is formed in one field of the chromium layer 102 containing the membrane 103. The conductive layer 108 is formed in the field of another side of the chromium layer 102. The conductive layer 108 is used when forming the chromium layer 102 with electrolysis plating. However, the conductive layer 108 is not the indispensable composition of the stencil mask 101, and it can also be removed after formation of the stencil mask 101 so that it may mention later.
[0047]When performing electron beam lithography of a package projection exposure method like PREVAIL or SCALPEL, the membrane 103 side of the stencil mask 101 of drawing 4 (a) is irradiated with the electron beam of about 100 keV, for example. The electron beam irradiated by the membrane 103 penetrates only aperture 107 portion to the strut 104 side by no being scattered about, and converges on resist. PREVAIL and SCALPEL(s) are usually 4 times as many reduction projection systems.
[0048]Next, the manufacturing method of the stencil mask 101 of this above-mentioned embodiment is explained below with reference to drawing 4 - 6. First, as shown in drawing 4 (b), silicon oxide is formed in one field of the silicon wafer 111 as the sacrificial film 112, and the conductive layer 108 is formed in the upper layer of the sacrificial film 112. As the silicon wafer 111, for example, it is used for manufacture of LSI, the wafer of 8 inch sizes can usually be used. The sacrificial film 112 is formed after formation of the stencil mask 101 the making the stencil mask 101 separate from the silicon wafer 111 easily purpose. As the conductive layer 108, a titanium layer is formed by vacuum evaporation etc. Electrical conducting materials other than titanium by which normal use is carried out by a semiconductor manufacturing process, such as tungsten, can also be used for the conductive layer 108.
[0049]Next, the resist 113 is formed in aperture 107 formation area on the conductive layer 108 as shown in drawing 4 (c). The resist 113 serves as a mold for forming the membrane 103 which has the aperture 107. The resist 113 scans and exposes the electron beam converged like the electron beam direct writing art in which it is used for the usual LSI manufacturing

process after applying resist to the whole surface, and can form it by developing negatives after that.

[0050]Next, as shown in drawing 5 (d), electrolysis plating of chromium is performed and the chromium layer 102a is formed on the conductive layer 108. In order to form the membrane 103 of uniform thickness, electrolysis plating of chromium is performed until the resist 113 is covered thoroughly. Here, the layer which consists of material in which plating of those other than chromium is possible may be formed instead of forming a chromium layer. Then, as shown in drawing 5 (e), the surface of the resist 113 is exposed by electrolytic polishing. Thereby, the chromium layer 102 which has an aperture into resist 113 portion is formed. This electrolytic polishing can be performed using the device used for electrolysis plating as it is.

[0051]Although electrolysis plating and electrolytic polishing were the art in which it was not used in the conventional LSI manufacturing process, since it comes to be adopted as a gold bump's formation and the damascene process of copper interconnect in recent years, they have been positively introduced also into manufacture of LSI. As a method for film deposition of a wiring material, physical vapor deposition (PVD;physical vapordeposition) or chemical-vapor-deposition methods (CVD;chemical vapor deposition), such as sputtering and vacuum deposition, were in use conventionally. However, it is necessary to perform membrane formation of the metallic material by these methods under vacuum, for example, to heat at about 200 **. Therefore, cost becomes high easily. Generally a reflow after membrane formation is also required.

[0052]On the other hand, processing at ordinary temperature is possible for electrolysis plating among the atmosphere, and, also technically, it has already reached the practical use level. A reflow after membrane formation is also unnecessary and membrane formation speed is also high as compared with PVD or CVD. Generally step coverage nature and the embedding characteristic of a viahole are also good as compared with PVD or CVD. Processing at ordinary temperature is possible also for electrolytic polishing among the atmosphere like electrolysis plating.

[0053]In manufacture of LSI, in order to solve the problem of the wiring delay accompanying the minuteness making of a device, lower-dielectric-constant-izing of an interlayer insulation film and low resistance-ization of the wiring material are advanced. The art which forms wiring in the insulator layer which consists of an organic system polymer material of a lower dielectric constant with electrolysis plating by this has also progressed.

[0054]For example, the embedding characteristic of the viahole of a high aspect ratio or the wiring material to a trench improves by optimizing a presentation, a speed of supply or electrode structure, current impression conditions, etc. of plating liquid. It is also possible to perform in the present electrolysis plating which uses resist as a mold using the embedded wiring art in manufacture of LSI.

[0055]After performing electrolysis plating and electrolytic polishing, the resist 114 is formed in the portion used as the membrane except the strut formation area on the chromium layer 102 as shown in drawing 5 (f). The high resolution like the lithography which forms the resist 113 by which minuteness making was carried out to aperture formation is not required of the lithography which forms the resist 114.

[0056]Therefore, a strut pattern can be transferred by the photolithography used for circuit pattern production of a mounting board, etc., for example. For example, it is specifically used by a mounting board etc., after applying thick film system resist, such as polyimide, the resist 114 is formed by performing exposure and development. The resist 114 is formed by thickness which becomes comparable as height h of a request of the strut 104 (refer to drawing 4 (a)).

[0057]Next, as shown in drawing 6 (g), after performing electrolysis plating of chromium, electrolytic polishing is performed succeedingly and chromium is embedded between the adjoining resist 114. Thereby, the strut 104 linked to the chromium layer 102 is formed considering the resist 114 as a mold. Electrolysis plating and electrolytic polishing for forming the strut 104 can be similarly performed using the same device as electrolysis plating of the chromium layer 102a and electrolytic polishing (refer to drawing 5 (d) and (e)) which use resist 113 as a mold.

[0058]Next, as shown in drawing 6 (h), the resist 114 and the resist 113 are removed. As shown in drawing 6 (i), aperture 107 portion of the conductive layer 108 formed in electrolysis plating is removed. Then, the stencil mask 101 shown in drawing 4 (a) is made to separate from the silicon wafer 111 by removing the sacrificial film 112. When silicon oxide is formed as the sacrificial film 112, the wet etching using fluoric acid can remove the sacrificial film 112, for example.

[0059]Instead of making the sacrificial film 112 and the conductive layer 108 which consist of silicon oxide as mentioned above laminate, the aluminum layer of a monolayer can be formed, for example and the function of both a sacrificial film and a conductive layer can also be given. In this case, although not illustrated, the chromium layer and strut which have an aperture are formed like the process shown in drawing 6 (h) from drawing 4 (b).

[0060]Then, if an aluminum layer is removed, the membrane which has an aperture will be formed and a stencil mask and a silicon wafer will dissociate. An aluminum layer is removable by the wet etching using the etching reagent which contains phosphoric acid (H_3PO_4), nitric acid (HNO_3), acetic acid (CH_3COOH), and water (H_2O), for example.

[0061]According to the manufacturing method of the mask of this above-mentioned embodiment, the dry etching process of a silicon wafer currently performed in the conventional mask manufacture becomes unnecessary. According to electrolysis plating, since membranes can be formed, TAT of strut formation can be shortened substantially in a short time.

[0062]According to the manufacturing method of the mask of this above-mentioned

embodiment, the mechanical strength of the membrane 103 is fully reinforced with the silicon wafer 111 until it makes the stencil mask 101 separate from the silicon wafer 111. Therefore, breakage of the mask in a mask manufacture process is prevented, and the yield of a mask improves.

[0063]An aperture and a strut are formed where the whole mask surface is stably supported with a silicon wafer by the manufacturing process of a mask. Therefore, process tolerance improves as compared with the conventional manufacturing method which performs etching and lithography, supporting mask original recording only by a strut. Therefore, the defect of a mask pattern decreases.

[0064]According to the manufacturing method of the mask of this above-mentioned embodiment, the aperture 107 is formed in the membrane 103 of electrolysis plating and electrolytic polishing. When forming an aperture by dry etching, the edge roughness of an aperture increases easily. Since good step coverage nature and embedding characteristic are acquired to it according to electrolysis plating, the edge roughness of an aperture is reduced and the defect of a mask pattern is reduced.

[0065]The manufacturing method of the semiconductor device of this embodiment produces a stencil mask in accordance with the manufacturing method of the mask of this above-mentioned embodiment, and uses the produced mask for electron beam lithography, such as PREVAIL. Since according to the manufacturing method of the semiconductor device of this embodiment TAT of mask manufacture is shortened and the yield of a mask improves, the manufacturing cost of a semiconductor device is reduced. Since the pattern processing accuracy of the mask for lithography is high, in an electron-beam-lithography process, a minute pattern can be transferred with high precision on a wafer.

[0066](Embodiment 2) Drawing 7 (a) is a schematic diagram of the stencil mask of this embodiment, and drawing 7 (b) is the perspective view which expanded a part of drawing 7 (a) (A). The stencil mask 121 of this embodiment is used for the electron beam lithography of a reduction projection system like SCALPEL, for example.

[0067]As shown in drawing 7 (a), the stencil mask 121 is formed, for example considering the wafer form chromium layer 102 of 8 inch sizes as a base. The chromium layer 102 contains two or more membrane parts (membrane) 103 with a size of 1 mm x 12 mm, for example. The membrane 103 is mutually separated by the beam called the strut 104. The width of the strut 104 between the membranes 103 is 300 micrometers. The neighborhood of an edge of the chromium layer 102 in which the membrane 103 is not formed is also thick-film-ized by the strut 104. The strut 104 acts as a base material which maintains the mechanical strength of the stencil mask 121.

[0068]As shown in drawing 7 (b), the thickness of the membrane 103 is 1 micrometer. According to the stencil mask 121 of this embodiment, the strut 104 is formed like the stencil

mask of Embodiment 1 using chromium. Therefore, the height of the strut 104 can be arbitrarily set up regardless of the thickness of a silicon wafer in the range in which the mechanical strength of the stencil mask 121 is maintained.

[0069]As for the membrane 103, an aperture is formed in a pattern space like the stencil mask of Embodiment 1 including the skirt board of a pattern space and its circumference. The section structure of the stencil mask of this above-mentioned embodiment is common in the stencil mask of Embodiment 1, and can manufacture the stencil mask of this embodiment in accordance with the manufacturing method of the mask shown in Embodiment 1.

[0070]The stencil mask for the electron beam lithography of an actual size projection system besides a stencil mask applicable to the above SCALPEL(s) can also be manufactured in accordance with the manufacturing method of the mask shown in Embodiment 1. As electron beam lithography of an actual size projection system, For example, RIPURU, LEEPL (low.) which Tokyo Seimitsu and Sony are developing jointly energy electron-beam. proximity projection lithography /T. Utsumi and Journal of Vacuum Science and Technology B17 p.2897 (1999) are mentioned.

[0071]The embodiment of a mask of this invention and a manufacturing method for the same, and the manufacturing method of a semiconductor device is not limited to the above-mentioned explanation. For example, it is also possible to apply the manufacturing method of the mask of above-mentioned this invention to manufacture of the mask for lithography using exposure means, i.e., X-rays, EUV light, or ion beams other than an electron beam, etc. In addition, it is a range which does not deviate from the gist of this invention, and various change is possible.

[0072]

[Effect of the Invention]According to the mask of this invention, it becomes possible to raise the efficiency of mask manufacture and to improve the process tolerance of a pattern. According to the manufacturing method of the mask of this invention, it becomes possible to raise the efficiency of mask manufacture and to improve the process tolerance of a pattern. According to the manufacturing method of the semiconductor device of this invention, the manufacturing efficiency and the yield of a semiconductor device can be raised by including the lithography process using the above-mentioned mask.

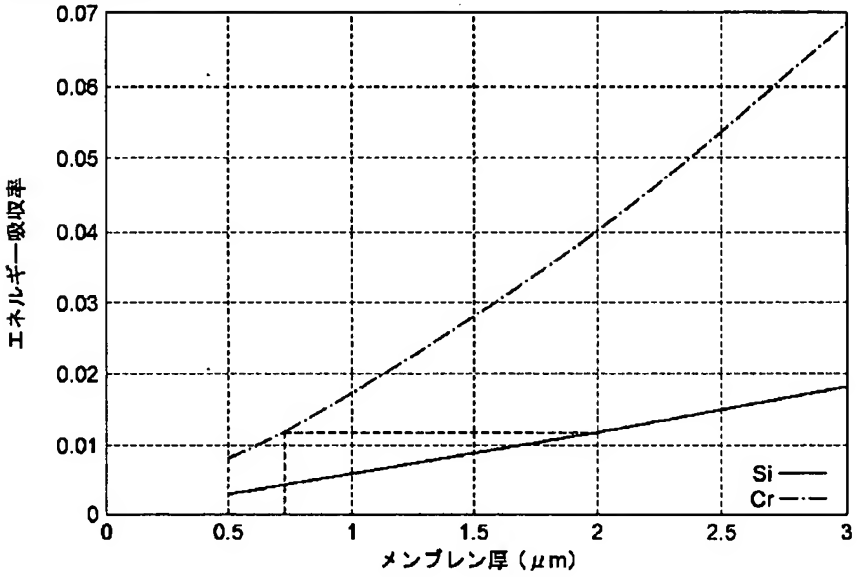
[Translation done.]

* NOTICES *

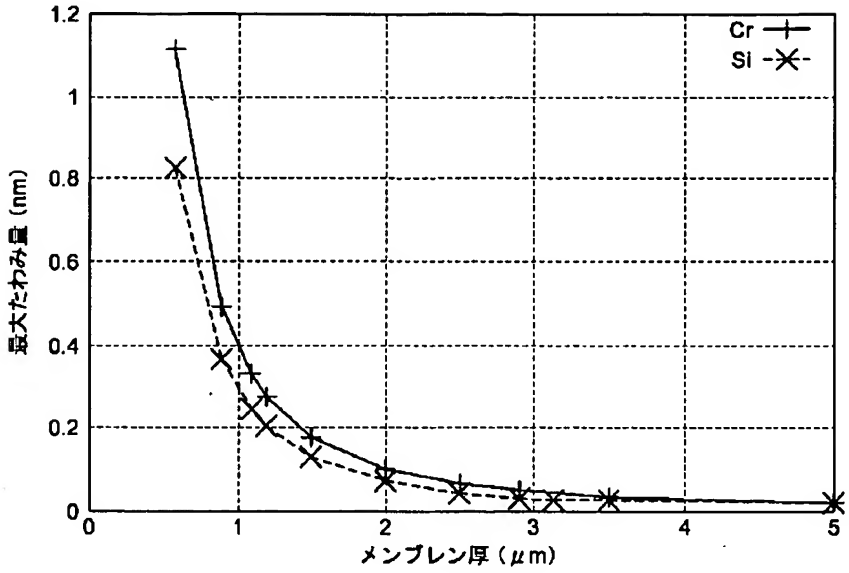
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

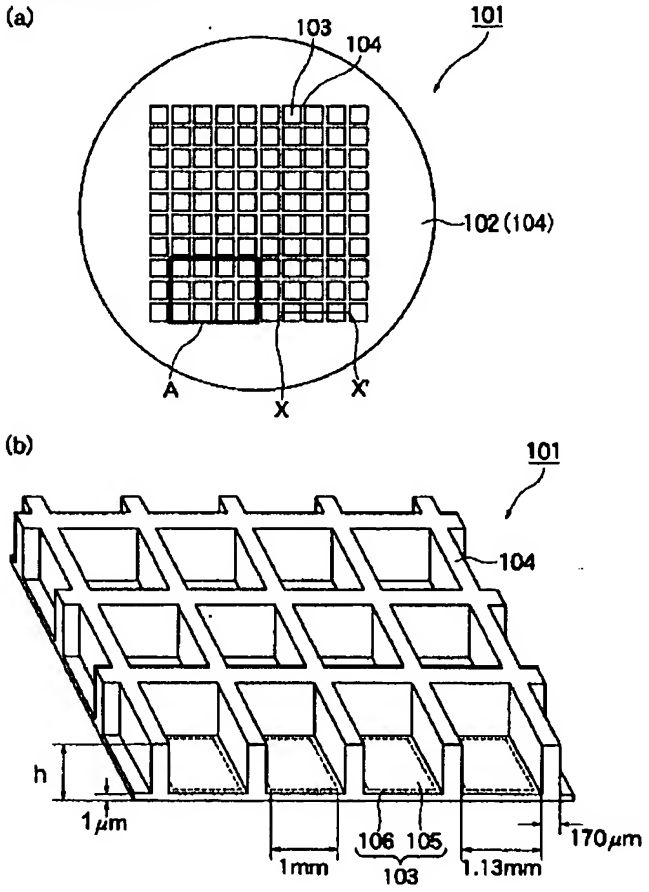
[Drawing 1]



[Drawing 2]

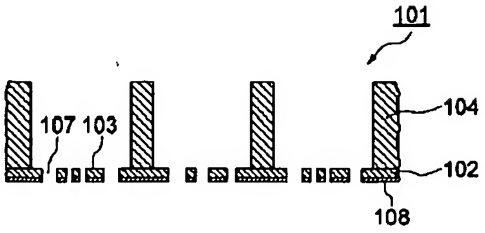


[Drawing 3]

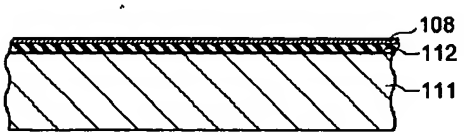


[Drawing 4]

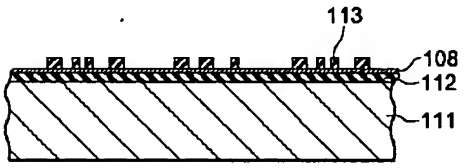
(a)



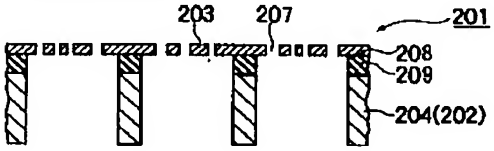
(b)



(c)

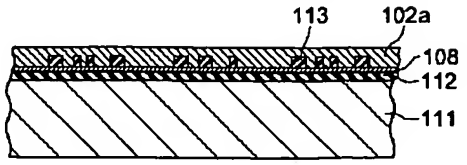


[Drawing 9]

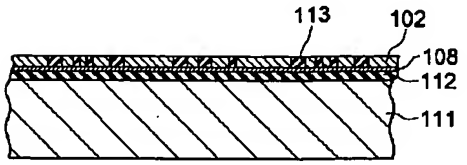


[Drawing 5]

(d)



(e)



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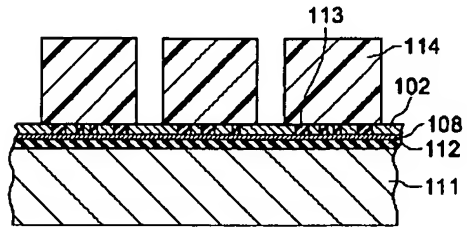
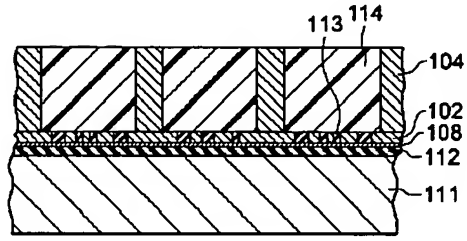
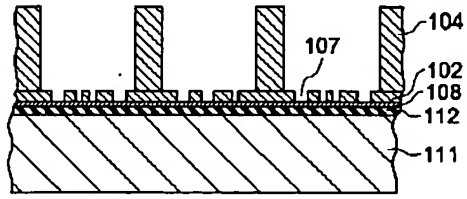


[Drawing 6]

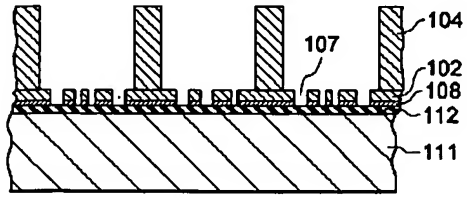
(g)



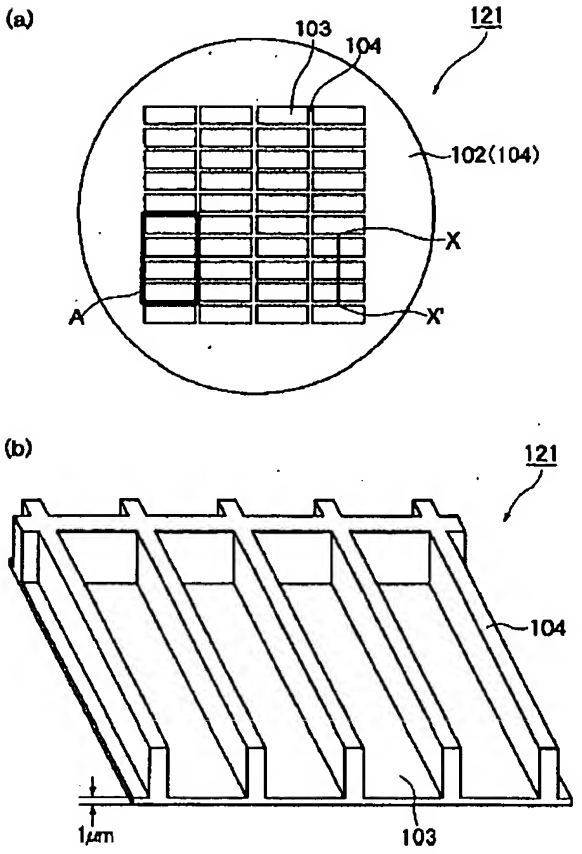
(h)



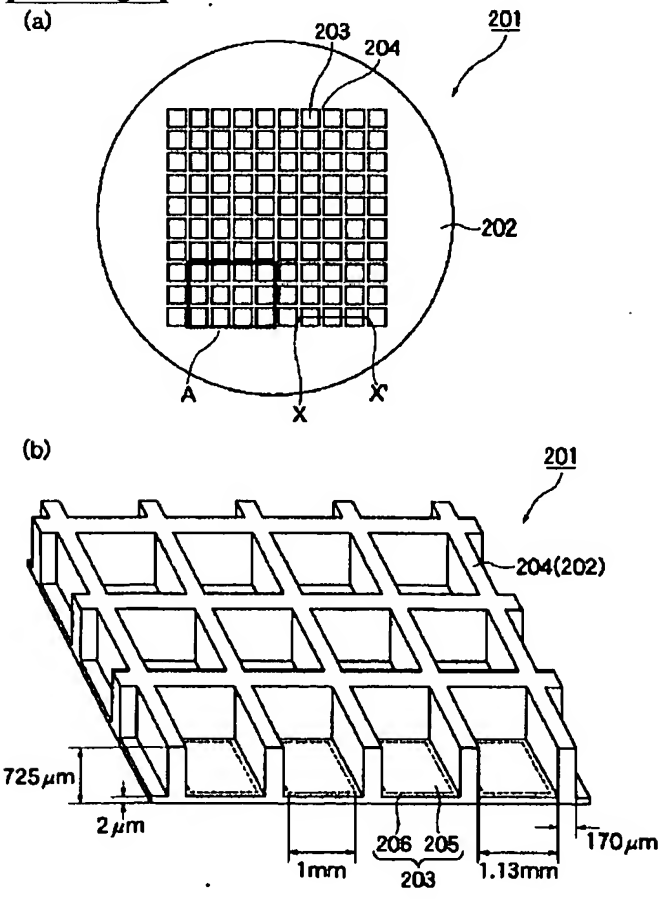
(i)



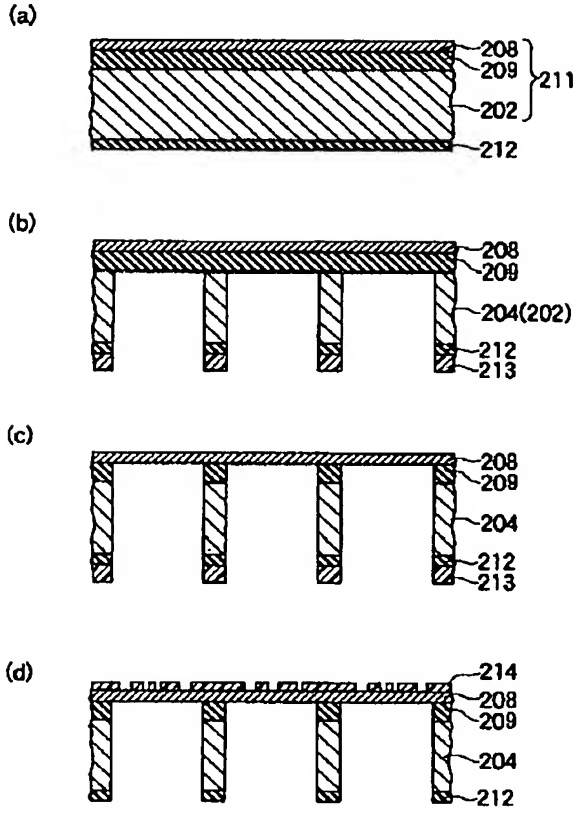
[Drawing 7]


(a)
103
104
121
102(104)
X
A
X'
(b)
121
104
1μm
103

[Drawing 8]


(a)
203
204
201
202
A
X
X'
(b)
201
204(202)
725μm
2μm
1mm
206 205
203
1.13mm
170μm

[Drawing 10]



[Translation done.]